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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/820,594 | 04/08/2004 | Yen-Fu Chiang | BCS03206 | 8117 |

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| EXAMINER | |
|---|---|
| JACKSON, BLANE J | |
| **ART UNIT** | **PAPER NUMBER** |
| 2618 | |

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/820,594 | CHIANG ET AL. | |
| | Examiner | Art Unit | |
| | Blane J. Jackson | 2618 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *27-30* are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☑ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election without traverse of claims 1-26 in the telecom with Mr. Ben Driscoll on 2 August 2006 is acknowledged.

### *Specification*

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 5-7, 14, 17 and 22 are rejected under 35 U.S.C. 102(e) as being anticipated by Kawakami et al. (US 2005/0122428).

As to claim 1, Kawakami teaches a radio frequency (RF) tuner comprising:

A tuner housing (figure 13, paragraph 0076, tuner (81), one of two shown mounted parallel to each other, comprising an EMI shielding structure including the walls, cover (212) and the ground plane (81B)),

A cover coupled to a first side of said housing (figure 13, paragraph 0076, tuner (81) with shield plate (212)),

A tuner printed circuit board including a plurality of layers coupled to a second side of said housing (figure 12A, paragraphs 0068-0069, double sided printed circuit board (21) comprises components mounted to the wiring side layer (81A) and the opposite board surface includes an overall conductive pattern or ground plane (81B) which is connected to a ground pattern of the component side surface and a frame-like or component wall shield plate (212). Also, an embodiment of a three layer PCB shown in figure 10, paragraphs 0058-0061, the PCB includes a component mount layer (13), a first ground layer (15) and a second ground layer (17)),

Wherein said layers are configured to shield said tuner PCB (figure 10 three layer embodiment, paragraph 0058 and 0065 and figure 13, a double sided PCB, paragraph 0075, ground surface (81B) acts as shield.

As to claim 5, Kawakami teaches the RF tuner of claim 1 wherein a bottom layer of said plurality of layers comprises a solid ground plane configured to form a shield (figure 10, paragraph 0061, second bottom ground layer (17) of three layers comprises a solid ground plane and figure 13, paragraph 0075, ground surface (81B) of double sided PCB of tuner (81)).

As to claim 6, Kawakami teaches the RF tuner of claim 1 further comprising a network connector communicatively coupled to said tuner PCB (figures 12A and 13, paragraphs 0070, 0076, connector (218)).

As to claim 7, Kawakami teaches the RF tuner of claim 6, wherein said network connector comprises a coaxial cable connector (paragraph 0070, antenna (coaxial RF connector) input connector (218)).

As to claim 14, Kawakami teaches a set-top box comprising:

A chassis (figure 9, paragraphs 0059-0061, set-top box (30)),

A tuner coupled to said chassis (figure 9, paragraph 0059tuner circuits 1 and 2 arranged parallel to each other),

A demodulator communicatively coupled to said tuner (figure 9, paragraph 0060, Demux (31)) and

A central processing unit (CPU) communicatively coupled to said demodulator (figure 9, paragraph 0060, CPU (34)),

Wherein said tuner includes a tuner housing, a cover coupled to a first side of said housing and a tuner printed circuit board (PCB) including a plurality of layers coupled to a second side of said housing wherein said layers are configured to shield said tuner PCB (figures 12A and 13, paragraphs 0068-0076, EMI shield structure

of tuner (81) comprising ground surface (81B) of double sided printed board (210), figure 3, paragraph 0016; frame-like walls (94) and shield plates (212),

As to claim 17, Kawakami teaches the set-top box of claim 14 wherein said tuner further comprises a vertical mount tuner (figure 13, paragraph 0073, two tuners (81) and (82) are shown and described as mounted to the main board, the ground surfaces (81B) and (82)B are parallel to each other and an RF connector of each tuner projects through a rear end panel (301) of the set-top box).

As to claim 22, Kawakami teaches a method of assembling an RF tuner comprising:

Coupling a tuner printed circuit board (PCB) to a first side of a tuner housing (figure 12A and 13, paragraph 0069 and 0076, a frame-like shield plate (212) meaning walls and cover) and

Coupling a tuner cover to a second side of said tuner housing (figure 13, paragraph 0069, tuner (81) and shield plate (212) the ground layer is connected to a ground pattern of the component layer and a frame-like shield plate (212) is provided on the component side surface, to the ground pattern),

Wherein said tuner PCB includes a plurality of layers configured to shield said tuner PCB (figure 13, paragraph 0075, a double sided board and figure 10, paragraphs 0061-0066, tuner (1) and triple sided PCB).

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 3, 11, 15, 16 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (US 2005/0122428) in view of Donaldson (US 4,370,515) and further in view of Yi et al. (US 2005/0042928).

As to claims 2, 11, 15 and 25 with respect to claims 1, 8, 14 and 23, Kawakami of Kawakami modified teaches the RF tuner of claim 1 wherein the tuner PCB further comprises a plurality of *finger connector pins* (figure 12A, pins (219) formed in the tuner PCB to electrically coupled the tuner PCB to a second PCB, paragraph 0074. However, Kawakami modified does not teach a plurality of *finger connector extrusions* formed in the tuner PCB to electrically coupled the tuner PCB to a second PCB.

Yi teaches a printed circuit card edge connector (1) which electrically couples a daughter PCB (6) with finger connector extrusions to a second or mother PCB (5), figure 1, paragraphs 0004-0008.

It would have been obvious to one of ordinary skill in the art to modify the signal pins of Kawakami modified with the PCB edge connector approach of Yi for simple and reliable connection of two printed circuit cards.

As to claim 3, Kawakami teaches the RF tuner of claim 2 wherein said tuner further comprises a vertical mount tuner (figure 13, figure 4, prior art and figure 13, paragraphs 0006, 0073, two tuners are taught mounted to the rear wall and coupled vertically to the main set-top box PCB).

As to claim 12, Kawakami teaches the RF tuner of claim 11 wherein said second PCB comprises a main PCB of a set-top box (figure 9, paragraphs 0059-0061, set-top box (30)).

As to claim 16, Kawakami teaches the set-top box of claim 15 wherein said second PCB comprises a main PCB of said set-top box (figure 13, paragraph 0073, tuner (81) is mounted to the main printed board (302)).

Claims 4, 8-10, 12, 18-20, 23, 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (US 2005/0122428) in view of Donaldson (US 4,370,515).

As to claims 4, 18 and 26, Kawakami teaches the RF tuner of claim 1, the set-top box of claim 14 and the method of claim 22 wherein said tuner housing further comprises a plurality of support members (figures 3 and 12A, frame like shield plates (94) although discussed for the prior art is seen as applicable in figure 12A and 13) and a shield cover, figure 13, shield plate (212), paragraph 0076, but is silent as to a plurality of extrusions, said extrusions being configured to extrude through a plurality of

corresponding orifices in said tuner PCB or a plurality of ribs configured to receive a corresponding plurality of clip tabs of the cover.

Donaldson teaches a shielding structure (102) having peripheral walls of sheet metal with tabs (106) extending into apertures of a printed circuit board (108), figures 10 and 11, column 5, line 34 to column 6, line 4. Donaldson also teaches a plurality of ribs configured to receive a corresponding plurality of clip tabs or spring clips of the cover, column 5, lines 54-66.

Since Kawakami teaches a plurality of support members and shield cover, it would have been obvious to one of ordinary skill in the art at the time of the invention to identify the attachment of the shield walls and cover to the PCB of Kawakami in the method of Donaldson to provide an inexpensive and electrically tight solution (Donaldson-column 1, line 50 to column 2, line 12) for bonding together the shield structure.

As to claims 8 and 19, Kawakami teaches the RF tuner of claim 1 and the set-top box of claim 14 wherein the tuner PCB further comprises:

A top layer, said top layer including a plurality of tuner components (figures 7 and 10, paragraph 0058, component mount layer (13)),

An intermediate layer, said intermediate layer including a major ground plane (paragraph 0058, first ground layer (15)),

A bottom layer, said bottom layer including a total ground plane (paragraph 0058, second ground layer (17)).

Kawakami teaches an intermediate ground plane layer but does not teach the intermediate layer includes a number of signal paths and direct current (DC) voltage lines.

Donaldson teaches a shielding structure formed integrally with a ground layer of a printed circuit board where the multilayer board optionally contains interconnecting circuit layers, figure 11, column 5, line 67 to column 6, line 40.

It would have been obvious to one of ordinary skill in the art at the time of the invention to realize the intermediate ground layer of Kawakami to include interconnecting circuits such as signal paths and direct current voltage lines as suggested by Donaldson to provide the necessary interconnecting circuits common to RF double sided boards.

As to claim 9, Donaldson of Kawakami modified teaches the RF tuner of claim 8 wherein the tuner PCB is coupled to the tuner housing adjoining the top layer and said housing (figure 10, column 5, lines 34-54, tabs (94) along the walls (90) for insertion into apertures (96) of the printed circuit board (86) and coupled to the PCB mechanically and by wave soldering to the top layer ground traces and plated through holes).

As to claims 10 and 20, Donaldson of Kawakami modified teaches the RF tuner of claim 8 and the set-top box of claim 19 further comprising a plurality of plated through holes disposed in said top layer, said intermediate layer and said bottom layer (figure 10, column 5, lines 34-54, tabs (94) along the walls (90) for insertion into apertures (96)

of the printed circuit board (86) and coupled to the PCB mechanically and electrically by wave soldering to the top layer ground traces and plated through holes).

As to claim 23, Kawakami teaches the method of claim 22 but does not teach coupling a tuner PCB to a first side of a tuner housing comprises inserting a plurality of extrusions of said tuner housing through a plurality of corresponding orifices in said tuner PCB and performing a solder reflow process on said plurality of extrusions.

Donaldson teaches a shielding structure including the ground plane of a printed circuit with the method of coupling a tuner PCB to a first side of a tuner housing comprises inserting a plurality of extrusions of said tuner housing through a plurality of corresponding orifices in said tuner PCB (figure 11, column 5, line 66 to column 6, line 25, peripheral walls of sheet metal with tabs (106) extending into apertures of the printed circuit board (108)) and performing a solder reflow process on said plurality of extrusions (column 6, lines 25-27, solder (124) is applied most conveniently by wave soldering).

It would have been obvious to one of ordinary skill in the art to recognize the assembly of the shielding structure of Kawakami can be accomplished by the approach of Donaldson (column 1, line 50 to column 2, line 11) as an inexpensive solution of providing an EMI shielding structure.

As to claim 24 with respect to claim 23, Kawakami teaches various components such as an IC are mounted on the wiring pattern, paragraph 0069, but does not teach

inserting a plurality of RF tuner components through said tuner PCB and securing said plurality of RF tuner components to said tuner PCB using said reflow process.

Donaldson teaches a shielding structure including the ground plane of a printed circuit with the method further comprising inserting a plurality of components through a PCB and securing the plurality of components and the shielding structure to the PCB using a reflow process, column 6, lines 20-27.

It would have been obvious to one of ordinary skill in the art at the time of the invention to assemble the RF tuner board of Kawakami in the method of Donaldson such that the shield structure and discrete components are conveniently soldered in the circuit board at the same time.

Claims 13 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kawakami et al. (US 2005/0122428) in view of Nishimura et al. (US 6,522,872).

As to claims 13 and 21, Kawakami teaches the RF tuner of claim 8 and the set-top box of claim 19 wherein said tuner components comprise a down converter VCO, figure 6, paragraphs 0054-0055 and 0059. Kawakami is silent as to an up-converter variable crystal oscillator.

Nishimura teaches a tuner circuit on a PCB within an EMI structure where the upconverter section and a down converter section are contained in separate respective shield portions of the tuner EMI structure, figures 1-3. Nishimura further teaches the upconverter (10) comprises a mixing circuit and a first PLL (111) and a first local oscillator (LO-1) and the down converter (20) includes a second PLL (21), a second

local oscillator circuit (LO-2) and a down converter mixing circuit (D-MIX), column 4, lines 5-25.

Since Nishimura further teaches, with respect to claims 8 and 19, the signal line of the IF section is provided on an internal layer of a multilayered substrate and the signal line is surrounded with grounded conductive material on the upper a lower layers as a shield to noise (column 9, lines 24-28, it would have been obvious to one of ordinary skill in the art at the time of the invention to realize in the RF circuits of Kawakami the EMI structure of Kishimura such that multiple conversion circuits are contained in separate chassis for noise suppression.

***Conclusion***

The prior art made of record and not relied upon but considered pertinent to applicant's disclosure includes: Gammon (US 5,847,938), Geiger et al. (4,689,825), Perkins et al. (US 2002/0075664), Wada (US 6,041,224), Ohyama et al. (US 4,404,617), Shmagin et al. (US 6,560,125), Perkins et al. (US 6,490,173), Ito et al. (US 4,325,103), Yamauchi et al. (US 2001/0048593) and Kubo et al. (US 5,355,532).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Blane J. Jackson whose telephone number is (571) 272-7890. The examiner can normally be reached on Monday through Friday, 9:00 AM-6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward Urban can be reached on (571) 272-7899. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BJJ